



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Darrell Rinerson, et al.

Attorney Docket No.: **P027.03.CIP2+**

Application No.: **10/665,882**

Examiner: Kraig, William F.

Filed: **September 19, 2003**

Art Unit: **2815**

Title: **Resistive Memory Device With A
Treated Interface**

Customer No.: 42958

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APPEAL BRIEF – PATENTS PER 37 C.F.R. §41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief in connection with the decision of the Examiner in
a Final Office action mailed **August 2, 2006**. It is respectfully submitted that the
present application has been twice rejected. Each of the topics required in an
Appeal Brief are presented herewith and labeled appropriately.

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(i) **Real Party In Interest**

The real party in interest is Unity Semiconductor Corporation, a company established under the laws of the State of Delaware and having a principle place of business at 250 North Wolfe Road, Sunnyvale, CA 94085, U.S.A.

(ii) **Related Appeals and Interferences**

There are no appeals or interferences currently known to Appellants, Appellants' legal representatives, or the assignee which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

(iii) **Status of Claims**

Claims 1 – 5, 8 – 14, and 19 – 31 are pending and have been twice rejected. Claims 6 – 7 and 15 – 18 are cancelled. The rejection of Claims 1 – 5, 8 – 14, and 19 – 31 is hereby appealed.

(iv) **Status of Amendments**

No amendments are filed concurrent with this Appeal Brief or subsequent to the Final Office Action mailed **August 02, 2006**.

(v) Summary of Claimed Subject Matter

Apellants' invention as claimed is summarized and explained below with reference numerals, specification page numbers, and drawing figure numbers indicating where the claim finds support in the specification and the drawings.

1. A resistive memory device comprising:

a conductive bottom electrode having a top surface (705; FIG. 7) [page 12, paragraph 0022] ;

a multi-resistive state element having a top surface and a bottom surface (710; FIG. 7) , the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode (710, 705; FIG. 7), the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance [page 5, paragraph 0007; page 21, paragraph 0047] ;

a conductive top electrode (715; FIG. 7) having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element (715, 710; FIG. 7), wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes [page 5, paragraph 0008; page 20, paragraph 0045] ;

a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element (715, 710; FIG. 7) [page 5, paragraph 0007] ; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element (705, 710; FIG. 7), at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface [page 5, paragraph 0007; page 8, paragraph 0010] , and

whereby the properties of the at least one interface are changed by the at least one treatment [page 5, paragraph 0007; page 8, paragraph 0010; page 22, paragraph 0051; page 23, paragraphs 0053-0055; page 24, paragraphs 0056-0057] .

2. The resistive memory device of claim 1, wherein:

the at least one treatment is an ion implant [pages 22-23, paragraph 0052].

3. The resistive memory device of claim 1, wherein:

the at least one treatment is an exposure to an anneal [page 23, paragraph 0053] .

4. The resistive memory device of claim 3, wherein:

the anneal is performed while the multi-resistive state element is formed [page 23, paragraph 0053] .

5. The resistive memory device of claim 1, wherein:

the at least one treatment is an exposure to a gas [page 23, paragraph 0055; page 24, paragraph 0056] .

8. The resistive memory device of claim 3, wherein:

the anneal is performed after the conductive bottom electrode is formed [page 23, paragraph 0053] .

9. The resistive memory device of claim 3, wherein:

the anneal is performed after the multi-resistive state element is formed [page 23, paragraph 0053] .

10. The resistive memory device of claim 3, wherein:
the anneal is performed after the conductive top electrode is formed [page 23, paragraph 0053] .
11. The resistive memory device of claim 5, wherein:
the exposure to the gas causes a chemical reaction in the multi-resistive state material [page 23, paragraph 0055; page 24, paragraph 0056] .
12. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the conductive bottom electrode is formed [page 23, paragraph 0055; page 24, paragraph 0056] .
13. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the multi-resistive state element is formed [page 23, paragraph 0055; page 24, paragraph 0056] .
14. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the conductive top electrode is formed [page 23, paragraph 0055; page 24, paragraph 0056] .
19. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element [page 23, paragraph 0055; page 24, paragraph 0056] .

20. The resistive memory device of claim 19, wherein:

an anneal process is a catalyst for the chemical reaction [page 23, paragraph 0055; page 24, paragraph 0056] .

21. The resistive memory device of claim 19, wherein:

an exposure to a gas is a catalyst for the chemical reaction [page 23, paragraph 0055; page 24, paragraph 0056] .

22. The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a plasma process [page 23, paragraph 0053] .

23. The resistive memory device of claim 22, wherein:

the plasma process is a plasma etch [page 23, paragraph 0053] .

24. The resistive memory device of claim 1, wherein:

both the bottom interface and the top interface are subject to a treatment, the treatments being different from each other [page 38, third sentence in the Abstract of the Disclosure] .

25. The resistive memory device of claim 1, wherein:

the at least one treatment is caused by re-sputtering [page 24, paragraph 0057] .

26. The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a bombardment by inert ions [page 24, paragraph 0057] .

27. The resistive memory device of claim 1, wherein:

the at least one treatment is caused by a laser treatment [page 23, paragraph 0053] .

28. A resistive memory device comprising:

a conductive bottom electrode having a top surface (705; FIG. 7) [page 12, paragraph 0022] ;

a multi-resistive state element having a top surface and a bottom surface (710; FIG. 7) , the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode (710, 705; FIG. 7) , the multi-resistive state element having at least one layer that is fabricated to be substantially crystalline and have a programmable resistance [page 5, paragraph 0007; page 21, paragraph 0047] ;

a conductive top electrode (715; FIG. 7) having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element (715, 710; FIG. 7) , wherein the resistance of the resistive memory device may be programmed by applying a first voltage having a first polarity across the conductive electrodes and reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes [page 5, paragraph 0008; page 20, paragraph 0045] ;

a top interface created by the direct physical contact between the bottom surface of the conductive top electrode and the top surface of the multi-resistive state element (715, 710; FIG. 7) [page 5, paragraph 0007] ; and

a bottom interface created by the direct physical contact between the top surface of the conductive bottom electrode and the bottom surface of the multi-resistive state element (705, 710; FIG. 7) , at least one of the top interface or the bottom interface includes a treatment primarily directed towards changing properties of the at least one interface [page 5, paragraph 0007; page 8, paragraph 0010] , and whereby the properties of the at least one interface are changed by the treatment [page 5, paragraph 0007; page 8, paragraph 0010; page 22, paragraph 0051; page 23, paragraphs 0053-0055; page 24, paragraphs 0056-0057] .

29. The resistive memory device of claim 28, wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be polycrystalline [page 21, paragraph 0047] .

30. The resistive memory device of claim 28, wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be a perovskite [page 21, paragraphs 0047-0048] .

31. The resistive memory device of claim 30, wherein:

the at least one interface that is subjected to the treatment is directed towards changing properties of the perovskite (935; FIG. 9) [page 8, paragraph 10; page 26, paragraph 0063; pages 29-30, paragraph 0075; page 38, third sentence in the Abstract of the Disclosure] .

(vi) **Grounds of Rejection to be Reviewed on Appeal**

A. Claims 1 – 5, 8 – 14, and 19 – 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,759,249 to Zhuang et al.

(vii) **Argument**

Relevant Law – Legal Basis for Anticipation under 35 U.S.C. §102

A claim is anticipated under 35 U.S.C. §102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Argument re Issue A

Claims 1 – 5, 8 – 14, and 19 – 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,759,249 to Zhuang et al. (*Zhuang* hereinafter). Appellants respectfully assert that for at least the reasons set forth below, Claims 1 – 5, 8 – 14, and 19 – 31 are not anticipated by *Zhuang*.

Appellants' Independent Claim 1 – Recites the Following:

1. A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one

interface, and whereby the properties of the at least one interface are changed by the at least one treatment.

Claim 1, thus recites a “multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance.” Furthermore, Claim 1 recites “a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element” and “a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element.” Additionally, Claim 1 recites “at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface.”

One of the definitive and well respected texts on semiconductor devices describes an interfacial layer between adjoining semiconductor materials as one that “will be assumed to have a thickness of a few angstroms” (see S.M. Sze, “Physics of Semiconductor Devices”, 2nd Edition, pp 271 – 272). Appellants urge that the definition set forth in Sze is one that is generally accepted and well understood by one of ordinary skill in the microelectronics art and aptly describes the top and bottom interfaces recited in independent Claims 1 and 28 at issue in the present appeal. Real world processing techniques result in a transition layer (i.e., an interfacial layer) between adjoining layers that is not infinitesimally small, but rather is a few angstroms thick.

On Page 3, paragraphs 1 – 5 of the Final Office Action mailed **August 02, 2006** (Final Office Action hereinafter), the Examiner asserts that Appellants’ recited structure of: **(a)** a multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance; **(b)** a top interface including at least one treatment primarily directed towards changing properties of the top interface, and

the top interface is change by the treatment; and/or (c) a bottom interface including at least one treatment primarily directed towards changing properties of the bottom interface, and the bottom interface is change by the treatment, are met by the cited sections of *Zhuang* (i.e., Fig. 1, Col. 3, Lines 13 - 33, and Col. 7, Lines 39 – 42 of Claim 18). Appellants respectfully disagree with the Examiner's assertion for the reasons set forth below.

Zhuang discloses the following:

Referring now to FIG. 1, ... A layer of platinum 14 is deposited on the silicon substrate, and, in the preferred embodiment ... **Multiple layers of PCMO are spin coated** onto platinum layer 14 to a desired thickness, ... After each layer of PCMO film is spin coated, the structure is baked and annealed for between about five minutes and twenty minutes prior to the next coating process ... **Typically, three layers of PCMO are deposited, although, the desired thickness may require between two and five layers.** After the final layer is coated and baked, the stack of the film is annealed at low temperature ... After the low temperature processing steps, **the PCMO film is no longer in a single crystal form. The processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a.** A top electrode 18 is fabricated of platinum, which is deposited through a shadow mask, resulting in platinum buttons on the upper surface of the device. ... Top platinum dots 18, PCMO layer 16 and bottom platinum layer 14 form a PCMO resistor.

(Col. 3, Lines 5 – 44, emphasis added)

Thus, a non-volatile resistor memory cell fabricated **with amorphous PCMO has been disclosed.** Amorphous PCMQ [sic] may be deposited by at low temperature. The thermal budget of amorphous PCMO is compatible with state-of-the-art ULSI integrated circuit processes as the electrode material is also commonly used in the state-of-the-art process.

(Col. 4, Lines 59 – 64, emphasis added)

18. A method of fabricating a variable resistance R-RAM device comprising:

... wherein said depositing a perovskite metal oxide thin film includes depositing a layer of amorphous perovskite metal oxide thin film, and

wherein said baking changes a portion of the amorphous perovskite metal oxide thin film into a crystalline layer; ...

(Claim 18, Col. 7, Lines 39 – 42, emphasis added)

Accordingly, *Zhuang* disclose an amorphous PCMO layer 16b and a bottom PCMO layer 16a. The layer 16b is in contact with top electrode 18 and the bottom layer 16a is in contact with bottom electrode 14. The bottom PCMO layer 16a may include nano-meter size crystals. Collectively the layers 16a and 16b are referred to as PCMO layer 16. Moreover, *Zhuang* discloses a baking step in Claim 18 (Col. 7, Lines 39 – 42) that results in changing a portion of the amorphous PCMO into a crystalline layer.

Appellants' Claim 1 recites in pertinent part that "the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance." The Examiner asserts that Claim 18, Col. 7, Lines 39 – 42 of *Zhuang* meets the above structural limitations of Appellants' Claim 1. However, Claim 18 of *Zhuang* discloses "said baking changes a portion of the amorphous perovskite metal oxide thin film into a crystalline layer." Appellants argue that an amorphous PCMO layer having only a portion thereof changed into a crystalline layer by baking does not meet the limitation of a substantially crystalline structure recited in Appellants' Claim 1. The "changes a portion" language of *Zhuang* does not read on the substantially crystalline structure recited in Appellants' Claim 1.

Moreover, the Examiner's assertion in regards to Claim 18 are contradicted in Col. 2, Lines 60 – 63 where *Zhang* discloses that "Because the PCMO is in an amorphous form, it does not require a very high temperature treatment ...", in Col. 3, Lines 34 – 37 where *Zhuang* discloses "After the low temperature processing steps, the PCMO film is no longer in a single crystal form. The processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a", and in Col. 4, Lines 59 – 64

where *Zhuang* discloses “Thus, a non-volatile resistor memory cell fabricated with amorphous PCMO has been disclosed. Amorphous PCMQ [sic] may be deposited by at low temperature.”

Accordingly, the PCMO layer 16 of *Zhuang* is not a substantially crystalline layer for several reasons. First, Fig. 1 of *Zhuang* clearly depicts PCMO layer 16 including the top amorphous PCMO layer 16b and bottom PCMO layer 16a. Second, the bottom layer 16a may include nano-meter sized crystals, but that does not result in the entire PCMO layer 16 being a substantially crystalline layer. Finally, Claim 18 of *Zhuang* discloses that the baking process changes only a portion of the PCMO layer 16 into a crystalline layer.

Consequently, the structural limitation of a “multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance” is not explicitly or inherently disclosed in the cited sections of *Zhuang*. Therefore, all of the claim limitations of Appellants’ Claim 1 are not explicitly or inherently disclosed in the cited sections of *Zhuang* and the Examiner has not established a prima facie case of anticipation of Appellants’ Claim 1.

The Examiner further asserts that the limitation of “at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface, and whereby the properties of the at least one interface are changed by the at least one treatment” as recited in Appellants’ Claim 1 are met by Col. 3, Lines 13 – 33 and Claim 18, Col. 7, Lines 39 -42 of *Zhuang*.

Zhuang discloses the following:

Multiple layers of PCMO are spin coated onto platinum layer 14 to a desired thickness, which, in the preferred embodiment, is between about 100 nm to 300 nm. After each layer of PCMO film is spin coated, the structure is baked and annealed for between about five minutes and twenty minutes prior to the next coating process. During the baking process, in an ambient atmosphere, the temperature is

progressively stepped up from about 100.degree. C. to about 250.degree. C. For instance, the structure may be initially heated to about 120.degree. C. for one minute, then heated to about 180.degree. C. for about one minute, and then heated to about 240.degree. C. for about one minute. The structure is then annealed in an oxygen atmosphere at a temperature of between about 400.degree. C. to 700.degree. C. for the remainder of the time. The structure is then cooled, and the next layer of PCMO film is formed by spin coating. Typically, three layers of PCMO are deposited, although, the desired thickness may require between two and five layers. After the final layer is coated and baked, the stack of the film is annealed at low temperature in the range of between about 400.degree. C. to 700.degree. C. for between about five minutes to three hours in an oxygen atmosphere.

(Col. 3, Lines 13 – 33)

Appellants argue that nowhere in the above cited section of *Zhuang* is there an explicit or inherent disclosure of an interfacial treatment primarily directed towards changing a property of an interface and a property of the interface is changed by the treatment. Appellants' Claim 1 describes a treatment that is "primarily directed" towards changing an interfacial property. In contrast, the above cited section of *Zhuang* is silent as to an interface and/or an interfacial property that is changed by the multiple spin coating and baking/annealing processes. The Examiner asserts that *Zhuang* discloses a top interface between layers 16 (i.e., 16b) and 18 and a bottom interface between layers 16 (i.e., 16a) and 14. However, the above cited section of *Zhuang* does not disclose that the spinning/baking/annealing process is primarily directed towards changing an interfacial property of the top or bottom interfaces. Furthermore, in Col. 3, Lines 34 – 37, *Zhuang* discloses that "After the low temperature processing steps, the PCMO film is no longer in a single crystal form. The processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a." Nothing in that section of *Zhuang* discloses a treatment primarily directed towards changing a property of the top interface between layers 16b and 18 or the bottom interface between layers 16a and 14.

Appellants contend that if the words “at least one treatment primarily directed towards changing properties of the at least one interface” are to have any meaning whatsoever, those words must exclude treatments that effect entire bulk films. Although the Appellants recognize that interfacial treatments are imprecise and physical limitations may cause a treatment to tangentially effect the layers above and below the interface, “primarily directed” is clearly intended to not include treatments that indiscriminately modify surrounding layers in their entirety. Paragraphs 0010 and 0051 of Appellants’ application disclose that the at least one treatment is directed towards the top and/or bottom interfaces and the treatment changes a property of the interface.

The Examiner also asserts that Claim 18 of *Zhuang* disclose at least one treatment primarily directed towards changing properties of the at least one interface.

Zhuang discloses the following:

18. A method of fabricating a variable resistance R-RAM device comprising:

... wherein said depositing a perovskite metal oxide thin film includes depositing a layer of amorphous perovskite metal oxide thin film, and wherein said baking changes a portion of the amorphous perovskite metal oxide thin film into a crystalline layer; ...

(Claim 18, Col. 7, Lines 39 – 42)

The above cited section of *Zhuang* discloses a baking step that “changes a portion of the amorphous perovskite metal oxide thin film into a crystalline layer.” (emphasis ours) However, the cited section does not explicitly or inherently disclose that the changed portion is located at the interfaces (i.e., the junction between layers 16a/18 and/or layers 16b/14) or that the baking step is a treatment primarily directed towards changing the properties of the interfaces and a property of the interfaces are in fact changed by the treatment.

Consequently, the structural limitation of “at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface, and whereby the properties of the at least one interface are changed by the at least one treatment” are not explicitly or inherently disclosed in the cited sections of *Zhuang*. Therefore, all of the claim limitations of Appellants’ Claim 1 are not explicitly or inherently disclosed in the cited sections of *Zhuang* and the Examiner has not established a prima facie case of anticipation of Appellants’ Claim 1.

For at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang* and Appellants’ Claim 1 is patentably distinct in view of *Zhuang* and is allowable.

Appellants’ Dependent Claim 2

For at least the reasons as argued above for independent Claim 1, Claim 2 is allowable at least as depending from allowable Claim 1. Claim 2 recites in pertinent part “the at least one treatment is an ion implant.” On Page 4 of the Final Office Action, the Examiner asserts in regard to Claim 2, that Zhang discloses at least one treatment that causes a change in crystal structure (i.e., modifies a solid surface) at the at least one interface. The Examiner further asserts that a claim to the at least one treatment being an ion implant is a product-by-process claim that is not accorded patentable weight so long as the final product of the claim is the same or obvious in view of *Zhuang*. To support this assertion, the Examiner cites *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The Examiner contends that the particular process of causing the change in crystal structure is therefore irrelevant given that the final product is anticipated by *Zhuang*.

Zhuang discloses the following:

After the low temperature processing steps, the PCMO film is no longer in a single crystal form. The processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a.

(Col. 3, Lines 34 – 37)

The Appellant respectfully disagrees with the Examiner's assertions for the following reasons. First, the above cited section of Zhuang is silent as to at least one treatment that is an ion implant. An explicit or inherent disclosure of ion implantation is not found in the cited section. Moreover, Appellants' claim language recites that the treatment is primarily directed towards an interface and the treatment changes a property of the interface. However, the cited section of Zhuang only discloses that the processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a. The cited section does not explicit or inherent disclose that the change in crystal structure (i.e., the nano-meter size crystals) resides at the interface between layers 16a/14 and that the change in crystal structure is the result of the low temperature processing step. Second, an ion implantation directed toward the top and/or bottom interface of Appellants' Claim 1 results in a change in the structure of the interface that are distinct from the structure of the material in the layers that adjoin the interface, that is, species of the implanted ion would primarily reside in region that defines the interface. Therefore, the ion implant imparts a distinctive structural characteristic to the interface and the structure implied by the ion implant ought to be considered by the Examiner when assessing the patentability of Appellants' Claim 2 in view of the cited sections of *Zhuang*. *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979), MPEP §2113

Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*.

Therefore, Appellants' Claim 2 is patentably distinct in view of *Zhuang* and is allowable.

Appellants' Dependent Claims 3 – 4 and 8 - 10

For at least the same reasons as argued above for independent Claim 1, Claim 3 is allowable at least as depending from allowable Claim 1. Claim 3 recites in pertinent part “the at least one treatment is an exposure to an anneal.” On Page 4 of the Final Office Action, in regards to Claim 3, the Examiner asserts that *Zhuang* anticipates an anneal in Col. 3, Lines 13 – 33. However, as argued above in regards to Claim 1, the anneal disclosed in the cited section effects an entirety of the bulk PCMO layer 16 and the anneal is not primarily directed towards changing a property of an interface (i.e., the junction between layers 16b/18 and/or 16a/14). Moreover, the cited section is silent as to an interface or a treatment that specifically alters the properties of the interface.

Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under 35 U.S.C. §102(e) in view of the cited sections of *Zhuang*. Therefore, Appellants' Claim 3 is patentably distinct in view of *Zhuang* and is allowable.

Claims 4, 8, 9, and 10 depend from Claim 3 and are also allowable for at least the reasons argued above for Claims 1 and 3. On Page 5 of the final Office Action the Examiner asserts that Col. 3, Lines 13 – 33 and Claim 18, Col. 7, Lines 45-51 of Zhang anticipate Claims 4, 8, 9, and 10. However, the cited sections of *Zhuang* do not explicitly or inherently disclose an anneal directed primarily at changing the properties of an interface and the interface is changed by the anneal. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under 35 U.S.C. §102(e) in view of the cited sections of

Zhuang. Therefore, Appellants' Claims 4, 8, 9, and 10 are patentably distinct in view of *Zhuang* and are allowable.

Appellants' Dependent Claims 5, 11 - 14

Claims 5 and 11 - 14 depend from Claim 1 and are also allowable for at least the reasons argued above for Claim 1. In regard to Claim 5, on Page 5 of the Final Office Action, the Examiner contends that Col. 3, Lines 13 – 33 of *Zhuang* anticipates the at least one treatment being an exposure to a gas. However, as argued above in reference to Claim 3, the cited section of *Zhuang* does not explicitly or inherently disclose an exposure to a gas primarily directed towards changing the properties of an interface.

In regard to Claim 11, on Page 6 of the Final Office Action, the Examiner contends that Claim 18, Col. 7, Lines 39 – 42 of *Zhuang* anticipate exposure to a gas causing a chemical reaction in the PCMO. Appellants respectfully submit that the cited section is silent as to a gas, a chemical reaction, or a resulting chemical reaction caused by the gas reacting to the PCMO. Instead, the cited section discloses that a baking step changes a portion of the amorphous PCMO into a crystalline layer. The Examiner also asserts that exposure to a gas causing a chemical reaction in the multi-resistive state material is a product-by-process claim and therefore is not afford patentable weight. For at least the same reasons argued above in reference to Claim 2, Appellants argue that the chemical reaction implies a structural change in the multi-resistive state material that imparts a distinctive structural characteristic to the interface.

In regards to Claims 12 - 14, for at least the same reasons argued above for Claims 5 and 11, the cited section of *Zhuang* (Claim 18, Col. 7, Lines 45 – 51) is silent as to an exposure to a gas causing a chemical reaction that alters a property of an interface, regardless of when the exposure to the gas occurs. Consequently, for at least the reasons argued above, Appellants contend the

Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claims 5 and 11 -14 are patentably distinct in view of *Zhuang* and are allowable.

Appellants' Dependent Claims 19 - 21

Claims 19 – 21 depend from Claim 1 and are also allowable for at least the reasons argued above for Claim 1. As for Claim 19, on Page 7 of the Final Office Action, the Examiner contends that the at least one treatment being caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element is not given patentable weight because it is a product-by-process claim. For at least the same reasons argued above in reference to Claim 2, Appellants argue that the chemical reaction between the electrodes and the multi-resistive state element implies a structural change in the interface between the multi-resistive state material and the electrodes that imparts a distinctive structural characteristic to the interface and is therefore a structural element that ought to be given patentable weight. In that Claims 20 and 21 depend from Claim 19, an anneal or an exposure to a gas to effectuate the chemical reaction also impart a distinctive structural characteristic to the interface and ought to be given patentable weight. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claims 19 - 21 are patentably distinct in view of *Zhuang* and are allowable.

Appellants' Dependent Claims 22-23

Claims 22 - 23 depend from Claim 1 and are also allowable for at least the reasons argued above for Claim 1. As for Claims 22 – 23, Appellants argue that the Examiner is wrong by asserting on Page 7 of the Final Office Action that a

treatment caused by a plasma process or a plasma etch should be a product-by-process claim and should not be accorded patentable weight. The Appellants contend that for at least the same reasons argued above for Claim 2, the plasma treatment results in a structural change at the interface. The end result of the plasma process or the plasma etch is that the interface between the multi-resistive state element and the electrodes is structurally altered resulting in a distinct structure that ought to be given patentable weight. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a *prima facie* case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claims 22 - 23 are patentably distinct in view of *Zhuang* and are allowable.

Appellants' Dependent Claim 24

Claim 24 depends from Claim 1 and is allowable for at least the reasons argued above for Claim 1. On Page 8 of the Final Office Action, the Examiner asserts that *Zhuang* discloses in Col. 3, Lines 13 - 33 a top interface (layers 16 and 18) and a bottom interface (layers 14 and 16) that are subjected to a treatment and the treatments are different from each other. The Appellants argue that the cited section is silent as to the top interface because nowhere in the cited section is the top electrode 18 mentioned. Therefore, there is no top interface because there is no layer on top of the layer 16. The cited section only discloses the bottom interface between layers 14 and 16. Furthermore, nowhere in the cited section is there an explicit or inherent disclosure of different treatments primarily directed towards changing the property of the top or bottom interfaces. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a *prima facie* case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claim 24 is patentably distinct in view of *Zhuang* and is allowable.

Appellants' Dependent Claim 25

Claim 25 depends from Claim 1 and is allowable for at least the reasons argued above for Claim 1. On Page 8 of the Final Office Action, the Examiner asserts that *Zhuang* discloses in Col. 3, Lines 13 -33 and Lines 62 – 65, at least one treatment caused by physical re-sputtering. First, Col. 3, Lines 13 -33 is silent as to “re-sputtering” and only discloses spin-coating, which according to *Zhuang* is the preferred fabrication method (Col. 3, Lines 65 – 66). Second in Col. 3, Lines 62 – 65, *Zhuang* discloses metal oxide sputtering as one conventional technique that can be used to fabricate the metal oxide thin film (i.e., the PCMO layer 16). The technique disclosed by *Zhuang* teaches how to deposit the PCMO on the bottom electrode 14, however; the cited section is silent as to the use of physical re-sputtering to treat an interface thereby changing a property of the interface.

Appellants further argue that the Examiner is confusing sputtering, which is a deposition technique for forming thin film layers, with physical re-sputtering, which is a totally different processing technique that is distinct from conventional sputtering and ought not to be confused with conventional sputtering. Even though both terms incorporate the word “sputtering” there are significant differences between the two processes that clearly distinguish one from the other. The claims are interpreted in light of the specification. Appellants contend that Paragraph 0057 of the application clearly distinguishes physical re-sputtering from conventional sputtering as set forth below.

Appellants' Paragraph 0057 Recites:

Another treatment method might be to expose the entire structure and/or a particular surface layer to a physical re-sputtering, typically by using Ar and/or O₂ or other inert gas plasma. Re-sputtering is a technique commonly used to clean-up surfaces. Since a new film is

not deposited when the plasma hits the surface in the sputtering chamber, it can be considered to be the opposite of sputtering.

Similarly, the surface can be exposed to an inert ion from an ion gun, bombarding the surface with accelerated inert ions, such as ionized Ar.

(Emphasis Ours)

Consequently, for at least the reasons argued above, Appellants' contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claim 25 is patentably distinct in view of *Zhuang* and is allowable.

Appellants' Dependent Claims 26 and 27

Claims 26 and 27 depend from Claim 1 and are allowable for at least the reasons argued above for Claim 1. For Claims 26 and 27, the Examiner asserts the same product-by-process argument, that is, at least one treatment comprising bombardment by inert ions or laser treatment is not accorded patentable weight. For at least the same reasons as argued above for Claim 2, Appellants argue that a laser treatment or a bombardment by inert ions that results in a structural change in the interface imparts a structural distinctiveness to the interface that ought to be given patentable weight. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claims 26 and 27 are patentably distinct in view of *Zhuang* and are allowable.

Appellants' Independent Claim 28 – Recites the Following:

28. A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having at least one layer that is fabricated to be substantially crystalline and have a programmable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be programmed by applying a first voltage having a first polarity across the conductive electrodes and reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the conductive top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the conductive bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes a treatment primarily directed towards changing properties of the at least one interface, and

whereby the properties of the at least one interface are changed by the treatment.

The Examiner, in his rejection of independent Claim 28, cites the same sections of *Zhuang* that were used by the Examiner to support his rejection of independent Claim 1. The Appellants' contend that for at least the same reasons argued above for independent Claim 1, all of the claim limitations set forth in

independent Claim 28 are not explicitly or inherently disclosed in the cited sections of *Zhuang*. Consequently, for at least the reasons argued above, Appellants' contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claim 28 is patentably distinct in view of *Zhuang* and is allowable.

Appellants' Dependent Claim 29

For at least the reasons as argued above for independent Claim 28, Claim 29 is allowable at least as depending from allowable Claim 28. The Examiner on Page 10 of the Final Office Action asserts that Zhuang discloses at least one layer 16 this is fabricated to be substantially crystalline (Claim 18, Col. 7, Lines 39 – 42) and is fabricated to be polycrystalline (Col. 2, Lines 53 - 54). For at least the same reasons as argued above for independent Claim 1, the PCMO layer 16 of *Zhuang* is not a substantially crystalline layer as recited in Claim 28 from which Claim 29 depends. First, Fig. 1 of *Zhuang* clearly depicts PCMO layer 16 including the top amorphous PCMO layer 16b and bottom PCMO layer 16a. Second, the bottom layer 16a may include nanometer sized crystals, but that does not result in the entire PCMO layer 16 being a substantially crystalline layer. Finally, Claim 18 of Zhuang discloses that the baking process changes only a portion of the PCMO layer 16 into a crystalline layer. Although Col. 2, Lines 53 – 54 of Zhuang discloses “A low temperature annealing process renders the PCMO thin film in a basic amorphous or polycrystalline structure,” one of ordinary skill in the art is not put on notice that the entire PCMO layer 16 is polycrystalline because Fig. 1 of *Zhuang* depicts a layer 16a which may contain nano-meter sized crystals (Col. 3, Lines 34 – 37) and a layer 16b that is amorphous.

In Col. 2, Lines 45 – 49 *Zhuang* discloses “The method of the invention includes forming a PCMO metal oxide thin film on a substrate by spin-coating. PCMO thin films are polycrystalline ...” but contradicts that statement in Col. 2, Lines 62 –

65 where it is stated that “Because the PCMO is in an amorphous form, it does not require a very high temperature treatment, and may be formed on a device bottom electrode, such as are used in state-of-the-art silicon integrated circuit processes. In addition, the amorphous PCMO material may be uniformly deposited over the full silicon wafer”. Similarly, in Col. 4, Lines 59 – 63 *Zhuang* discloses “Thus, a non-volatile resistor memory cell fabricated with amorphous PCMO has been disclosed. Amorphous PCMQ [sic] may be deposited by at low temperature. The thermal budget of amorphous PCMO is compatible with state-of-the-art ULSI integrated circuit processes ...”. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants’ Claim 29 is patentably distinct in view of *Zhuang* and is allowable.

Appellants’ Dependent Claim 30

For at least the reasons as argued above for independent Claim 28, Claim 30 is allowable at least as depending from allowable Claim 28. In the rejection of Claim 30 the Examiner asserts on Page 11 of the Final Office Action, that *Zhuang*, in Col., Lines 15 – 20 and Col. 3, Lines 13 – 33, discloses a substantially crystalline layer 16 that is fabricated to be a perovskite. However, as argued above in reference to Claim 1, Appellants’ contend that the perovskite layer 16 (i.e., layers 16a and 16b) of *Zhuang* is not a substantially crystalline layer because at least a portion of the layer 16 is amorphous (i.e., layer 16b). Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants’ Claim 30 is patentably distinct in view of *Zhuang* and is allowable.

Appellants' Dependent Claim 31

For at least the reasons as argued above for independent Claim 30, Claim 31 is allowable at least as depending from allowable Claim 31. On Page 11 of the Final Office Action the Examiner asserts that *Zhuang* Col. 7, Lines 39 – 42 discloses a treatment directed towards changing properties of a perovskite. However, Appellants argue that the cited section of *Zhuang* does not disclose a treatment that changes the properties of an interface between the perovskite and an electrode in contact with the perovskite. As argued above in regards to Claim 1, the cited section of *Zhuang* discloses changing a portion of an amorphous perovskite into a crystalline layer and does not disclose a treatment primarily directed towards changing a property of an interface. Consequently, for at least the reasons argued above, Appellants contend the Examiner has not met his burden in proof in establishing a prime facie case of anticipation under **35 U.S.C. §102(e)** in view of the cited sections of *Zhuang*. Therefore, Appellants' Claim 31 is patentably distinct in view of *Zhuang* and is allowable.

Conclusion

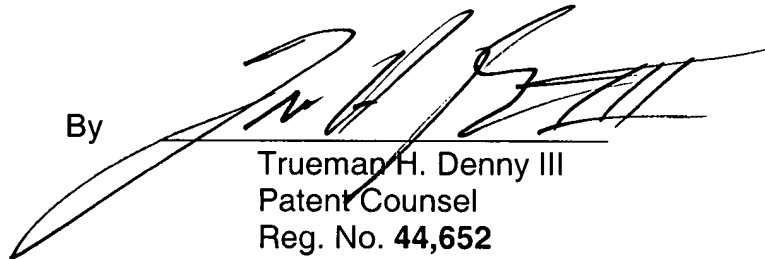
For at least the reasons given above, the rejection of Claims 1 – 5, 8 – 14, and 19 – 31 are improper. Accordingly, it is respectfully requested that such rejections by the Examiner be reversed and the pending claims be allowed. Attached below for the Board's convenience is an Appendix of Claims 1 – 5, 8 – 14, and 19 – 31 as currently pending.

Please grant any required extensions of time and charge any additional fees due in connection with this Appeal Brief to Unity Semiconductor Corp.
Deposit Account Number 50-3904.

Respectfully submitted,

Dated: February 20, 2007

By



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(viii) Claims Appendix

1. A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface, and

whereby the properties of the at least one interface are changed by the at least one treatment.

2. The resistive memory device of claim 1, wherein:

the at least one treatment is an ion implant.

3. The resistive memory device of claim 1, wherein:
the at least one treatment is an exposure to an anneal.
4. The resistive memory device of claim 3, wherein:
the anneal is performed while the multi-resistive state element is formed.
5. The resistive memory device of claim 1, wherein:
the at least one treatment is an exposure to a gas.
6. - 7. (Cancelled)
8. The resistive memory device of claim 3, wherein:
the anneal is performed after the conductive bottom electrode is formed.
9. The resistive memory device of claim 3, wherein:
the anneal is performed after the multi-resistive state element is formed.
10. The resistive memory device of claim 3, wherein:
the anneal is performed after the conductive top electrode is formed.
11. The resistive memory device of claim 5, wherein:
the exposure to the gas causes a chemical reaction in the multi-resistive state material.

12. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the conductive bottom electrode is formed.
13. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the multi-resistive state element is formed.
14. The resistive memory device of claim 5, wherein:
the exposure to the gas is performed after the conductive top electrode is formed.
15. - 18. **(Cancelled)**
19. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element.
20. The resistive memory device of claim 19, wherein:
an anneal process is a catalyst for the chemical reaction.
21. The resistive memory device of claim 19, wherein:
an exposure to a gas is a catalyst for the chemical reaction.
22. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by a plasma process.

23. The resistive memory device of claim 22, wherein:
the plasma process is a plasma etch.
24. The resistive memory device of claim 1, wherein:
both the bottom interface and the top interface are subject to a treatment,
the treatments being different from each other.
25. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by re-sputtering.
26. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by a bombardment by inert ions.
27. The resistive memory device of claim 1, wherein:
the at least one treatment is caused by a laser treatment.

28. A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having at least one layer that is fabricated to be substantially crystalline and have a programmable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be programmed by applying a first voltage having a first polarity across the conductive electrodes and reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the conductive top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the conductive bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes a treatment primarily directed towards changing properties of the at least one interface, and

whereby the properties of the at least one interface are changed by the treatment.

29. The resistive memory device of claim 28, wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be polycrystalline.

30. The resistive memory device of claim 28, wherein:

the at least one layer that is fabricated to be substantially crystalline is fabricated to be a perovskite.

31. The resistive memory device of claim 30, wherein:

the at least one interface that is subjected to the treatment is directed towards changing properties of the perovskite.

(ix) Evidence Appendix

None.

(x) Related Proceedings Appendix

None.